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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/124,288 07/28/98 BARRENSCHEEN

J GR-98-P-2078

EXAMINER

LM01/0412

LERNER AND GREENBERG
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WINDER, P

ART UNIT

PAPER NUMBER

2758

DATE MAILED:

04/12/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.
09/124,288

Applicant(s)

Barrenscheen et al.

Examiner

Patrice L. Winder

Group Art Unit

2758



☒ Responsive to communication(s) filed on Jul 28, 1998

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) 1-22 is/are pending in the application

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-4, 6, 12, and 19-22 is/are rejected.

☒ Claim(s) 5, 7-11, 13-18, and 22 is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☒ The drawing(s) filed on Jul 28, 1998 is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 4

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

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DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed August 24, 1998 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. (Note the examiner has only received a copy of the cover page of the cited reference.)

Drawings

2. The drawings are objected to because in figures 1-4 suitable meaningful legends (not numbers from the specification, "1", "3", "4") are required for inadequately labeled drawings (e.g. see MPEP 608.02 and 37 C.F.R 1.84(p)). Suggestion "MEM" for "1" Correction is required.
3. The drawings are objected to because the views of Figure 3, i.e. parts (a) - (d), should be relabeled Fig. 3(a), Fig. 3(b), Fig. 3(c) and Fig. 3(d), respectively. (See MPEP 608.02 and 37 CFR 1.84(p)). Correction is required.

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Claim Objections

4. Claim 22 is objected to because of the following informalities: the abbreviation "CAN" has not defined before use in the claim language. See MPEP 608.01(m) which illustrates appropriate orientation of abbreviations in the claims. Appropriate correction is required.

Specification

5. The disclosure is objected to because of the following informalities: the Brief Description of the Drawings does not reference parts (a) - (d) of Figure 3, see paragraph 3 above.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-4, 6, 12, 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leger, U.S. Patent No. 5,732,286 (hereafter referred to as Leger) in view of Klingelhofer, U.S. Patent No. 5,884,099 (hereafter referred to as Klingelhofer).

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8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

9. As to claim 1, Leger taught in a data transmission system with at least two subscribers (host CPU 101 and several external devices, col. 4, lines 48-57), a memory device to be connected (RAM based FIFO 208 of peripheral hardware controller 103, col.6, lines 1-6), for serial data transfer of binary data objects of a predetermined data width (serial data transfer of packets, col. 1, lines 52-54, composed of entities, col. 5, lines 57-58), between the at least two subscribers (serial I/O between the host CPU and the external devices, col. 5, lines 1-2), comprising:

a multiplicity of memory objects (RAM based FIFO 208 composed of 32- entity wide memory slots, col. 10, lines 27-30);

each said memory object having a data width being at least as large as a predetermined data width of a data object intended for data transfer (FIFO width = size of entity, col. 5, lines 60-62);

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at least one FIFO structure containing a plurality of said memory objects (RAM based FIFO, col. 6, lines 1-6) and transmitting data in a data-controlled data transfer controlled by the data objects being transmitted (data transfer controlled by monitoring marking tags of data packets, i.e. data controlled data transfer, col. 6, lines 32-33, col. 7, lines 48-53, 25-34).

Leger does not specifically teach memory objects being identifiable by a respective address. However, Klingelhofer taught memory object being identifiable by a respective address (identifiable address in input counter, col. 4, lines 21-27, col. 7, lines 56-59). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated Klingelhofer's identifiable address in Leger's FIFO buffering system because doing so would have improved system performance by providing a mechanism to indicate the present memory location being written or read. The motivation would have been because Klingelhofer's input counter offers an efficient mechanism to correlate a memory location to a specific address of the FIFO.

10. As to dependent claim 2, Leger taught wherein said memory objects are equal in size (width of the FIFO for the 32 byte depth is the size of an entity, col. 5, lines 62-65).

11. As to dependent claim 3, Leger's invention does not specifically teach wherein the subscribers in the data transmission system are operated at mutually different data transmission rates. However, Leger taught subscribers in the data transmission system are operated at mutually different data transmission rates (FIFOs are used to buffer time independent transmitters and receivers, i.e. subscribers, col. 1, lines 20-26). It would have been obvious to one of ordinary skill in the art at the time the invention was made that incorporating subscribers operated at mutually

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different transmission rates would improved the usability of Leger's system. The motivation would have been to provide another application in its field of use.

12. As to dependent claim 4, Leger taught wherein each of the subscribers is adapted to be a data transmitter and a data receiver (Inherent, the peripheral hardware controller controls data flows between the CPU system bus and external I/O devices. With respect to the external devices the peripheral hardware controller buffers data transmitted to and received from the serial I/O channels, col. 5, lines 1-7, i.e. the devices connected on either side of the peripheral controller are adapted to send and receive, col. 5, lines 35-44).

13. As to dependent claim 6, Leger taught wherein each of said FIFO structures has a data-controlled FIFO fill-level register indicating how many of said memory objects in said FIFO structure have already been written to and/or which are empty (up-down counter 703, col. 7, lines 48-53, 63-65).

14. As to dependent claim 12, Leger taught a method of operating the memory device which comprises:

defining a first operating mode wherein the following method steps are performed (first operating mode = external device is a sender and the host CPU is a receiver):

(a) providing a FIFO structure (RAM based receive FIFO);

(b) defining the first subscriber as a data transmitter and successively writing, with the data transmitter, a plurality of data objects to successively arranged memory objects in the FIFO structure (packets 0-4 are successively written to the FIFO, see fig. 6, col. 6, lines 51-53);

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(c) repeating the writing step until all the memory objects in the FIFO structure have been written to or all the data objects intended for data transfer have been stored in respective memory objects in the FIFO structure (writing = receiving packets into the FIFO until the entire FIFO depth is full, col. 5, lines 65-67);

(d) releasing the FIFO structure for a read operation (signaling the transmitting device to stop transmitting, col. 7, lines 25-30); and

(e) defining the second subscriber as a data receiver reading, with the data receiver, the data objects that have just been written to the respective memory objects in the FIFO structure (when the receive FIFO is full, i.e. the host CPU has been defined as the receiver, col. 6, line 65 - col. 7, line 3, lines 12-17), in a same sequence as they were written in the writing step (Inherent, by definition a FIFO is data transfer device where the first object in is the first object out. Hence the name first in first out (FIFO)).

15. As to dependent claim 19, Leger taught a method which comprises holding off with reading the memory objects that have been written to until after a request signal from a central processing unit or from the data receiver (request signal = number of free system memory buffers, col. 7, lines 15-19, col. 8, lines 22-25).

16. As to dependent claim 21, Leger taught wherein the first subscriber is a central processing unit (host CPU 101, col. 4, lines 48-50) and the second subscriber is coupled to a data bus of a bus system (the actual external devices are connected to the corresponding external interface, col. 4, lines 53-57).

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17. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leger and Klingelhofer as applied to claim 1 above, and further in view of Parks et al., U.S. Patent No. 5,623,700 (hereafter referred to as Parks).

18. As to dependent claim 20, Leger taught the at least two subscribers are bus systems and the memory device is connected between the subscribers (RAM based FIFO memory connects CPU system interface bus 104 with the bus systems of the external devices, such as the bus system of the SCSI interface, col. 4, lines 46-57). Leger does not specifically teach wherein the memory device is integrated in a bridge module. However, Parks taught a memory device is integrated in a bridge module (taught a bus bridge module within a peripheral controller connecting a host processor to external devices, col. 7, lines 38-56) . It would have been obvious to one of ordinary skill in the art at the time the invention was made that substituting Parks' bridge module for Leger's peripheral controller would have been an equivalent substitution. The motivation would have been Parks's bridge module forms an interface between a SCSI device and a host computer through its system bus likewise does Leger's peripheral controller.

19. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leger and Klingelhofer as applied to claim 21 above, and further in view of Gotze et al., U.S. Patent No. 5,941,966 (hereafter referred to as Gotze).

20. As to dependent claim 22, Leger taught a bus system comprising at least one memory device according to claim 1 (see claim 1 above). Leger does not specifically teach the bus system is a CAN bus system. However, Gotze taught a CAN bus system comprising a FIFO memory

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device (col. 4, lines 8-18, col. 5, lines 27-32). It would have been obvious to one of ordinary skill in the art that substituting Gotze's CAN bus system for Leger's bus system would have increased system usability. The motivation would have been to increase the available fields of use for Leger's controller.

Allowable Subject Matter

21. Claims 5, 7-11, 13-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

22. The following is a statement of reasons for the indication of allowable subject matter:

As to dependent claim 5, the prior art of record fails to teach or suggest each (emphasis added) memory object including an identification region which contains the address of the respective memory location;

As to dependent claims 7-8, the prior art of record fails to teach or suggest each memory object (emphasis added) including a node selection register designating which subscriber has been assigned the respective memory object;

As to dependent claim 9-10, the prior art of record fails to teach or suggest each memory object (emphasis added) of the plurality of memory objects including a gateway register which defines the operating mode of the respective memory object;

As to claim 11, allowable for the reasons given above for claims 7-10; and

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As to dependent claims 13-14, 16 and 18, the prior art of records fails to teach another operating mode for transferring data using two memory objects, comprising the steps of writing data to a first memory object; copying data from the first memory object to the second memory object and reading the data from the second memory object.

As to dependent claims 15 and 17, the prior art of record fails to teach or suggest another operating mode for transferring data using a single memory object.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kawauchi, U.S. Patent No. 5,619,653: taught a buffer device comprising: write attribute flags which are provided for a corresponding data holder in the buffer device and which indicate whether data is stored in the corresponding data holder and a read pointer which designates the read sequence of data taken from the data holders;

Yeung et al., U.S. Patent No. 5,931,926: taught an interface circuit between a host computer system operating at a first clock and a computer network system operating at a second clock, the interface comprising first and second FIFO buffers for transferring data between the buss systems;

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Kalkunte, U.S. Patent No. 5,859,980: taught a network interface which transmits data packets between a host computer and a network, which includes a FIFO buffer memory wherein the data packets being transferred include addressing information;

Krantz et al., EPA 0 419 067 A2: taught a universal asynchronous receiver transmitter (UART) with a receive FIFO buffer and a transmit FIFO buffer;

Smyers, WO 97/33230: taught an asynchronous data pipe (ADP) for automatically managing asynchronous data transfers between an application and a bus structure, the ADP includes a register file that holds parameters controlling the data transfers and corresponding FIFO is used for the data transfer;

Eltrich, U.S. Patent No. 5,748,923: taught a CAN (controller area network) interface for periodic transmission of data between control devices interconnected through a serial bus;

Smith, U.S. Patent No. 4,965,794: taught a telecommunications FIFO which provides a interface between two serial data transmission channels operating at independent clocks, the FIFO contains two storage registers equal to a frame of data in length;

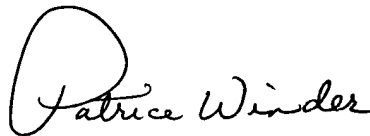
Liu et al., U.S. Patent No. 5,987,554: taught a method of controlling the transfer of information across an interface between two buses wherein the interface is a CAN interface that includes a FIFO memory;

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrice Winder whose telephone number is (703) 305-3938. The examiner can normally be reached on Monday-Friday from 7:30 AM to 4:00 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ahmad Matar, can be reached on (703) 305-4731. The fax phone number for this Group is (703) 308-9052.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

A handwritten signature in cursive script that reads "Patrice Winder". The signature is written in black ink and is positioned above the printed name and title.

Patrice Winder
Patent Examiner
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